

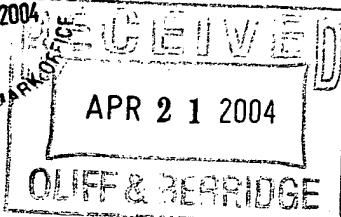


## UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
 United States Patent and Trademark Office  
 Address: COMMISSIONER FOR PATENTS  
 P.O. Box 1450  
 Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/623,495	07/22/2003	O I P E 1038		116637	9	36	1

25944  
 OLIFF & BERRIDGE, PLC  
 P.O. BOX 19928  
 ALEXANDRIA, VA 22320



CONFIRMATION NO. 6345

## FILING RECEIPT



\*OC000000012385471\*

Date Mailed: 04/19/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

## Applicant(s)

Cambridge, ENGLAND;

Takeo Kawase, Tokyo, JAPAN;

## Assignment For Published Patent Application

SEIKO EPSON CORPORATION, Tokyo, JAPAN;

## Domestic Priority data as claimed by applicant

## Foreign Applications

UNITED KINGDOM 0217425.8 07/26/2002

If Required, Foreign Filing License Granted: 11/25/2003

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Patterning Method  
Circuit fabrication method